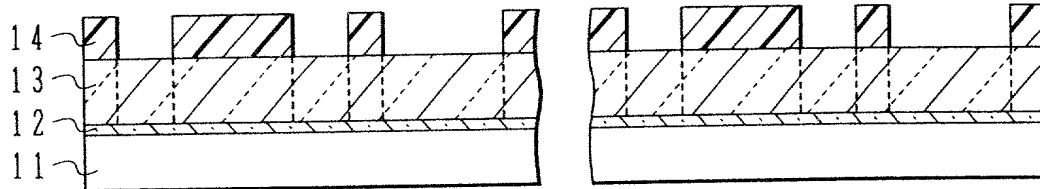


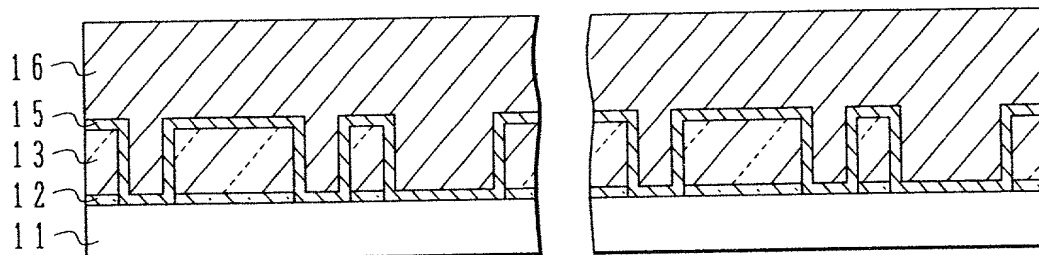
EFFECTIVE WAFER AREA

NONEFFECTIVE WAFER AREA  
(PERIPHERAL WAFER AREA)

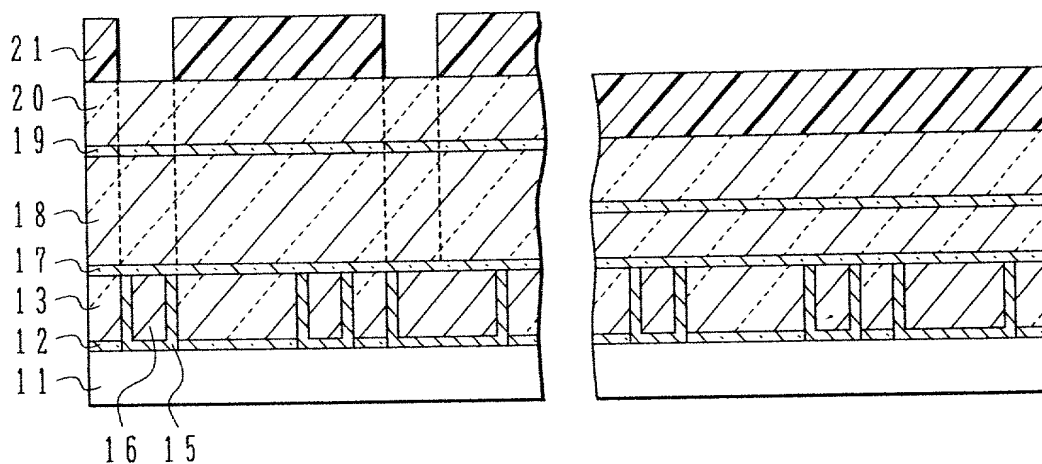
**FIG.1A**



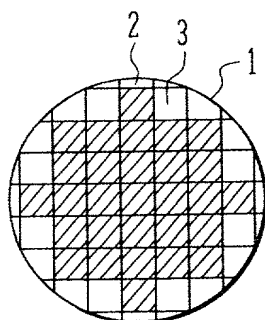
**FIG.1B**



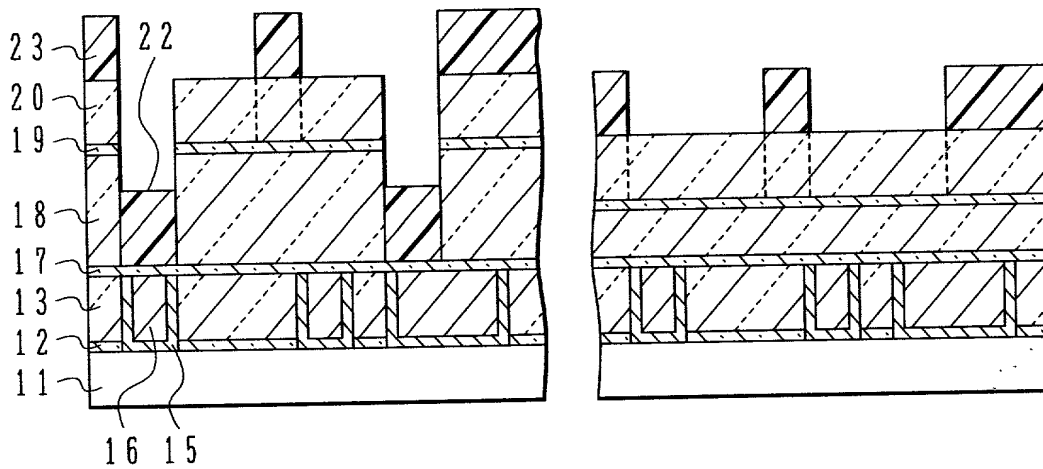
**FIG.1C**



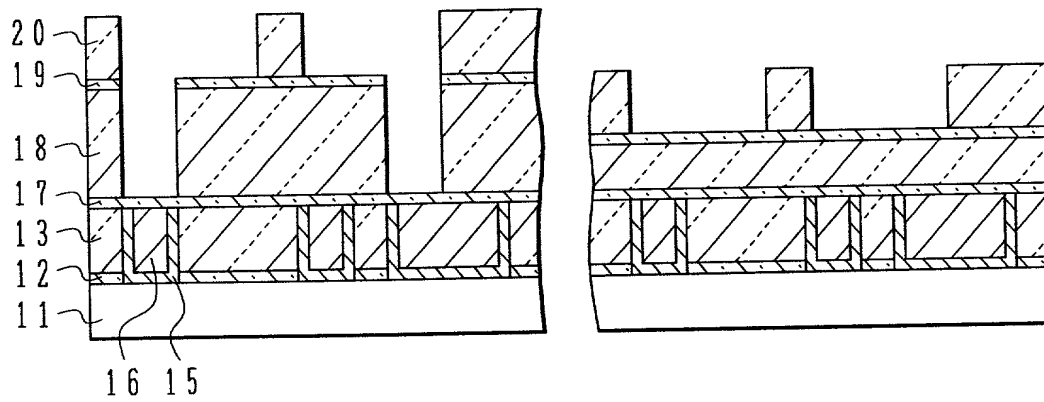
**FIG.1D**



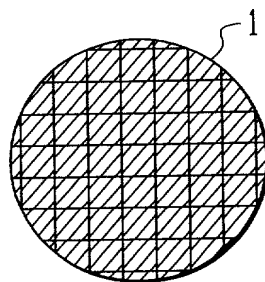
**FIG.1E**



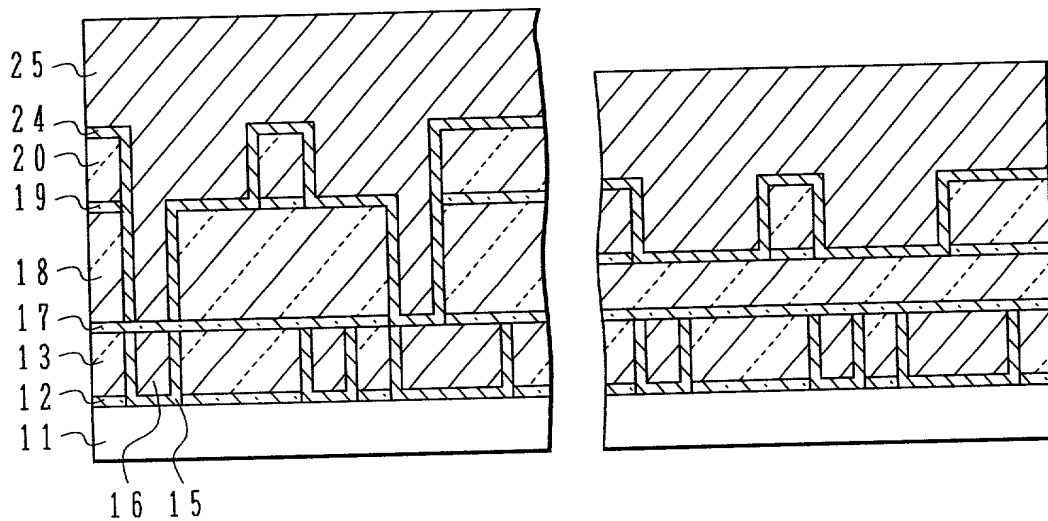
**FIG.1F**



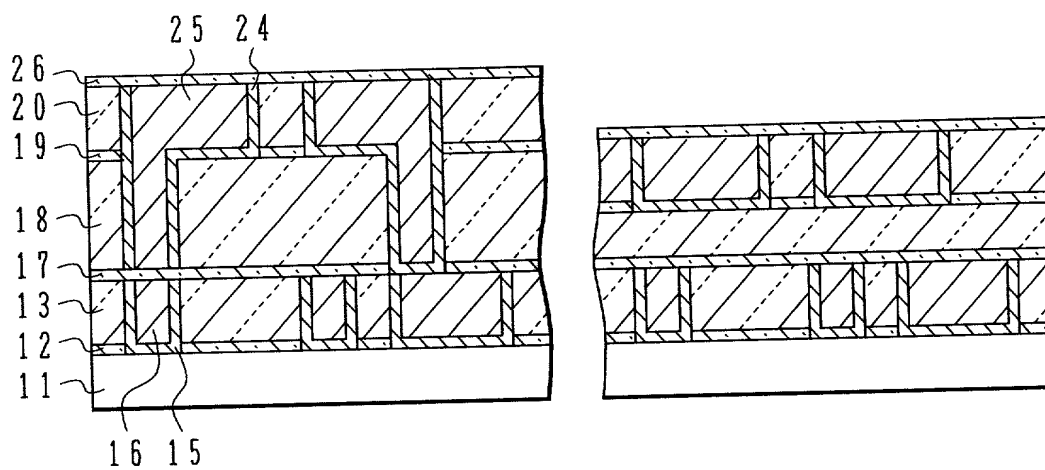
**FIG.1G**



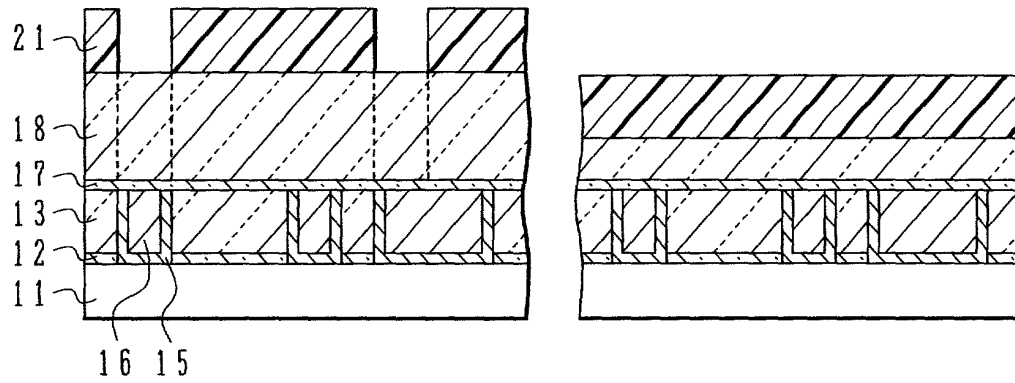
**FIG.1H**



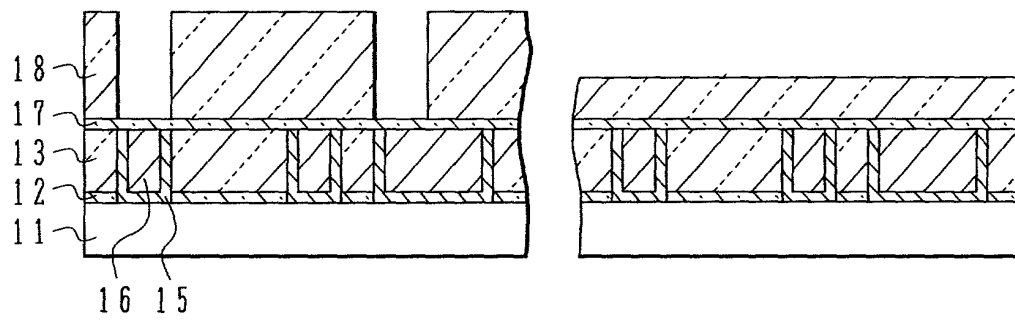
**FIG.1I**



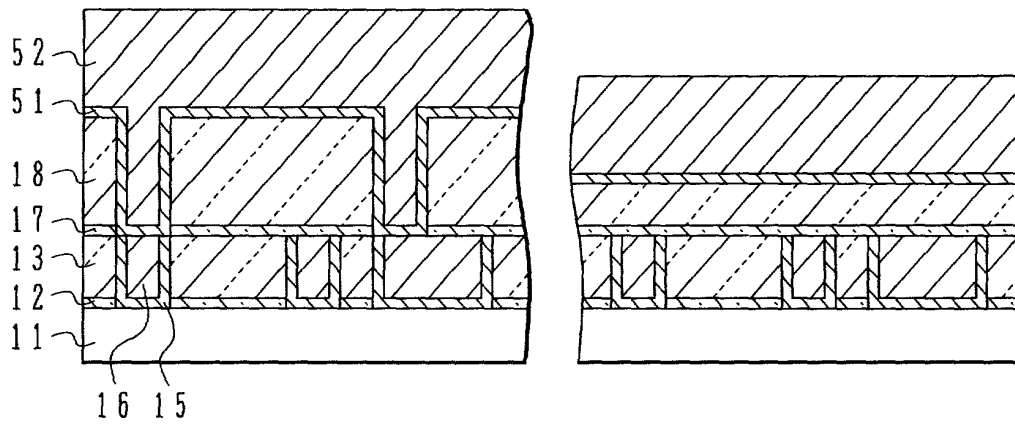
**FIG. 2A**



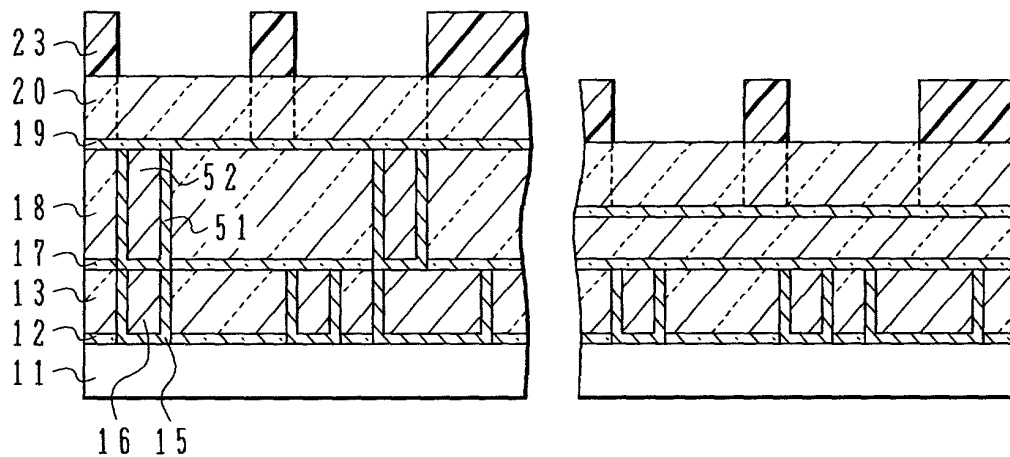
**FIG. 2B**



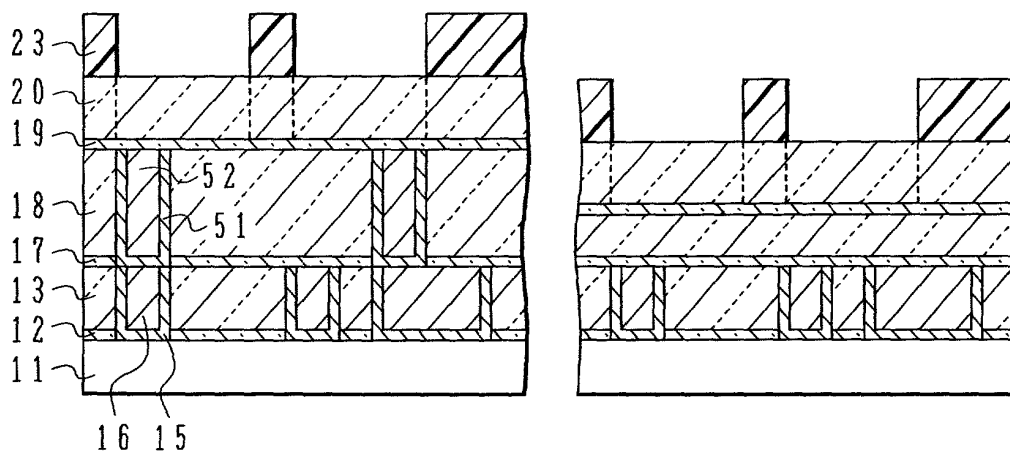
**FIG. 2C**



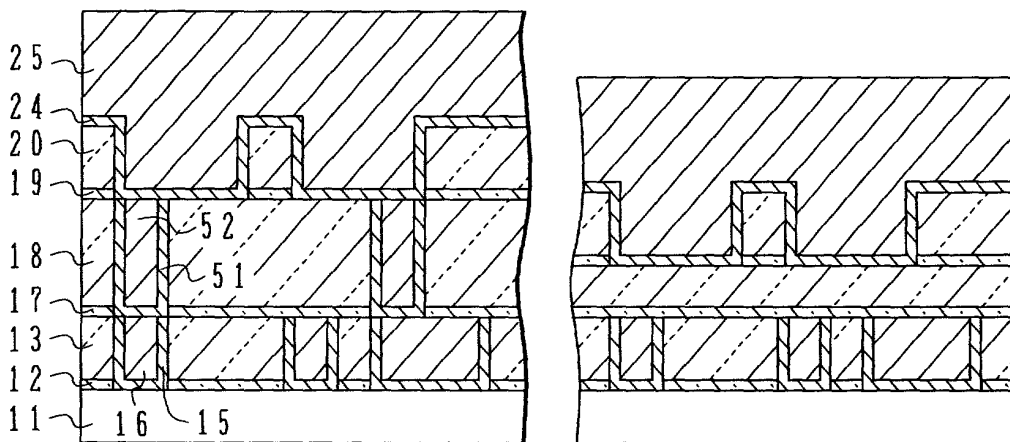
**FIG.2D**



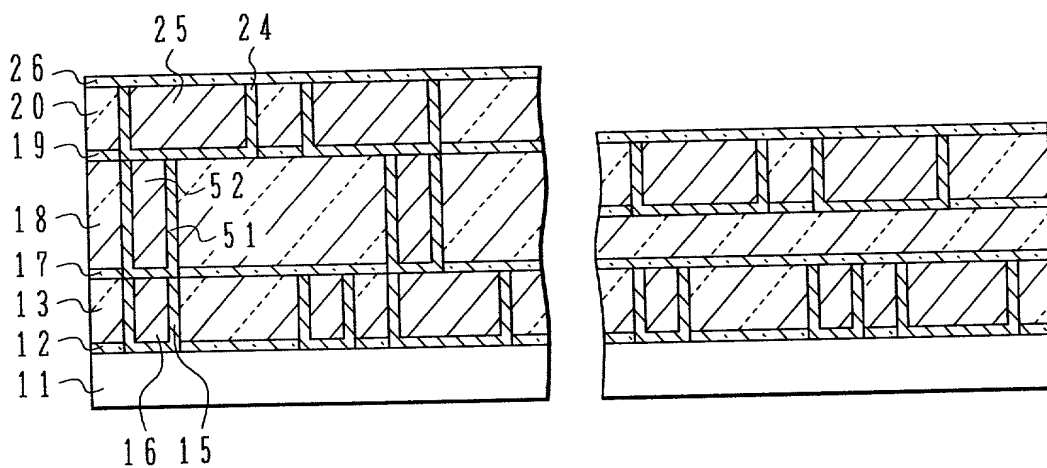
**FIG.2E**



**FIG.2F**



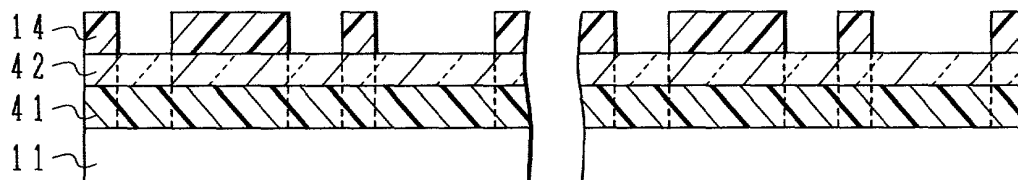
**FIG.2G**



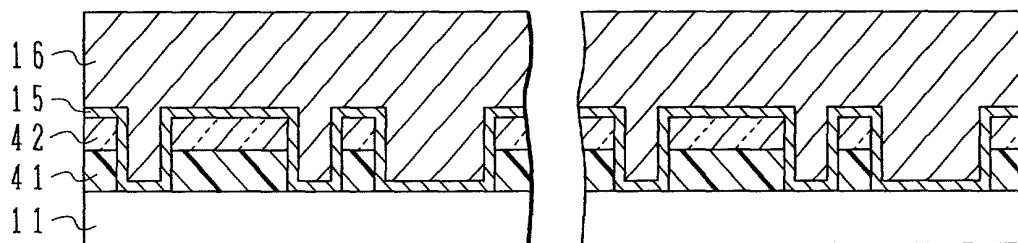
EFFECTIVE WAFER AREA

NONEFFECTIVE WAFER AREA  
(PERIPHERAL WAFER AREA)

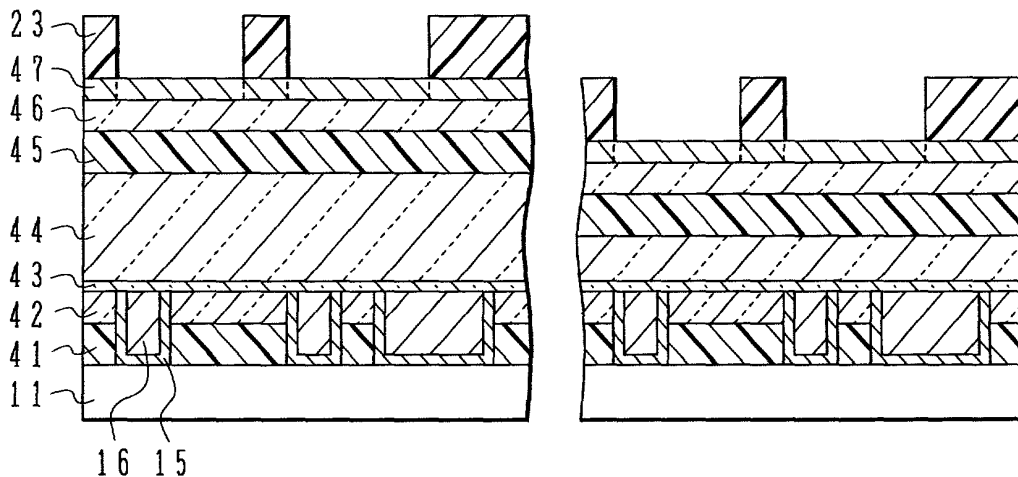
**FIG.3A**



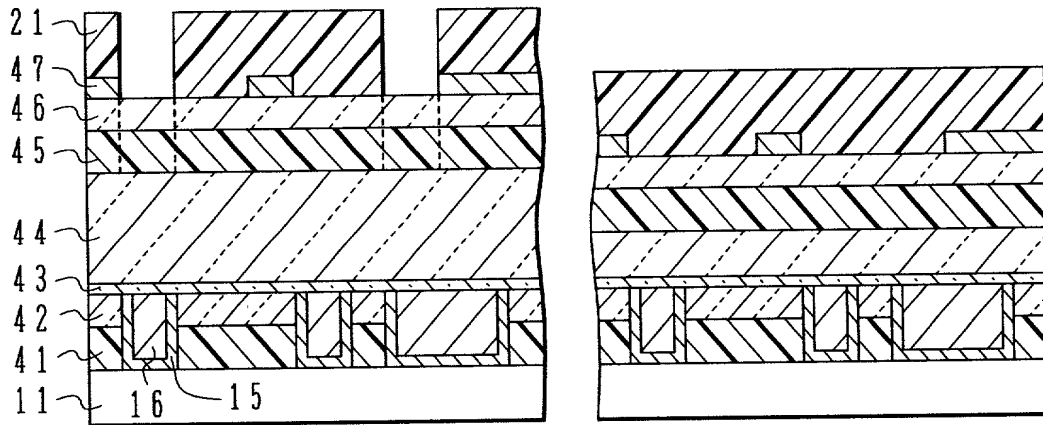
**FIG.3B**



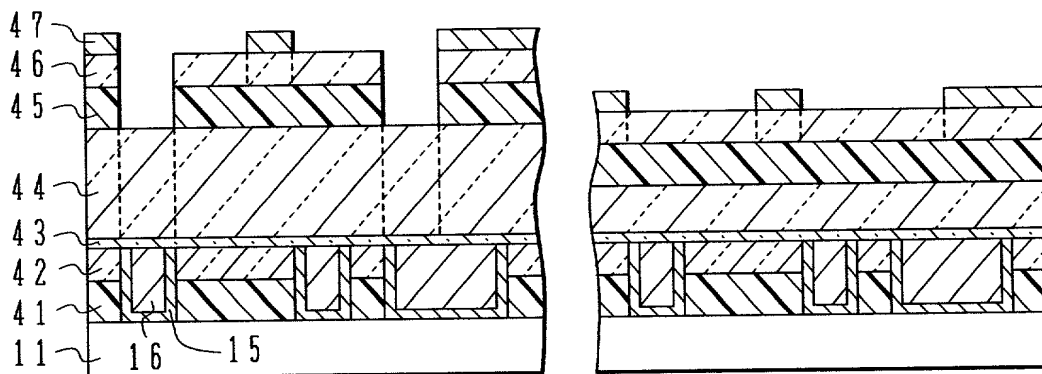
**FIG.3C**



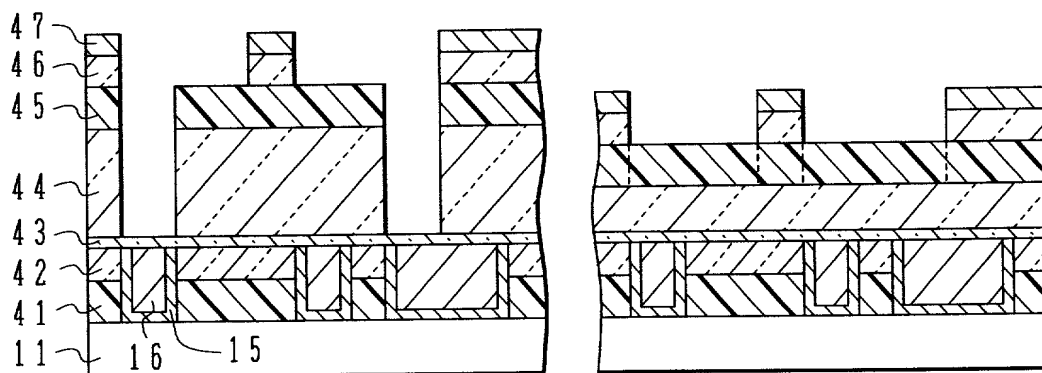
**FIG.3D**



**FIG.3E**

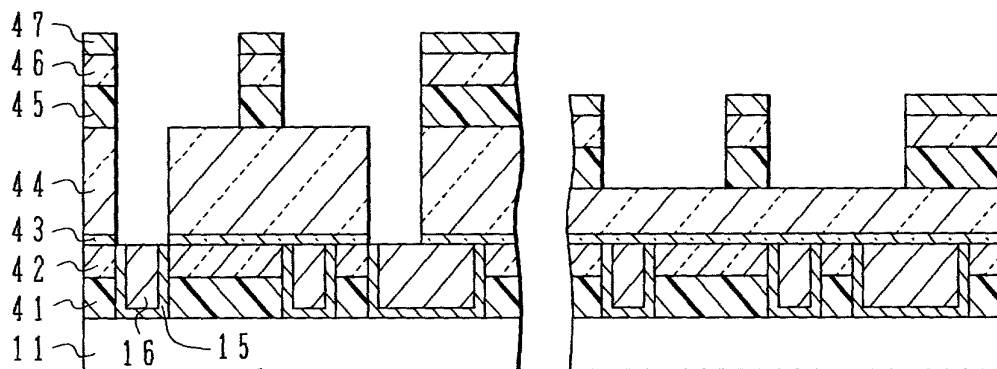


**FIG.3F**

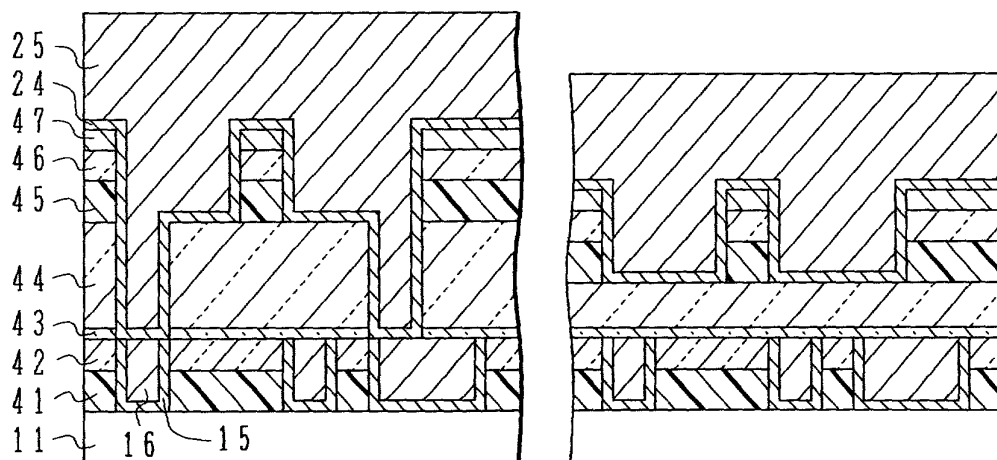




**FIG.3G**



**FIG.3H**



**FIG.3I**

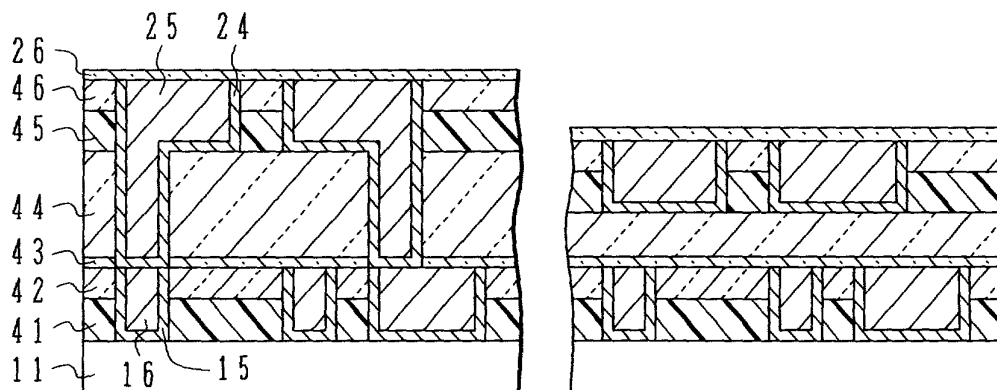
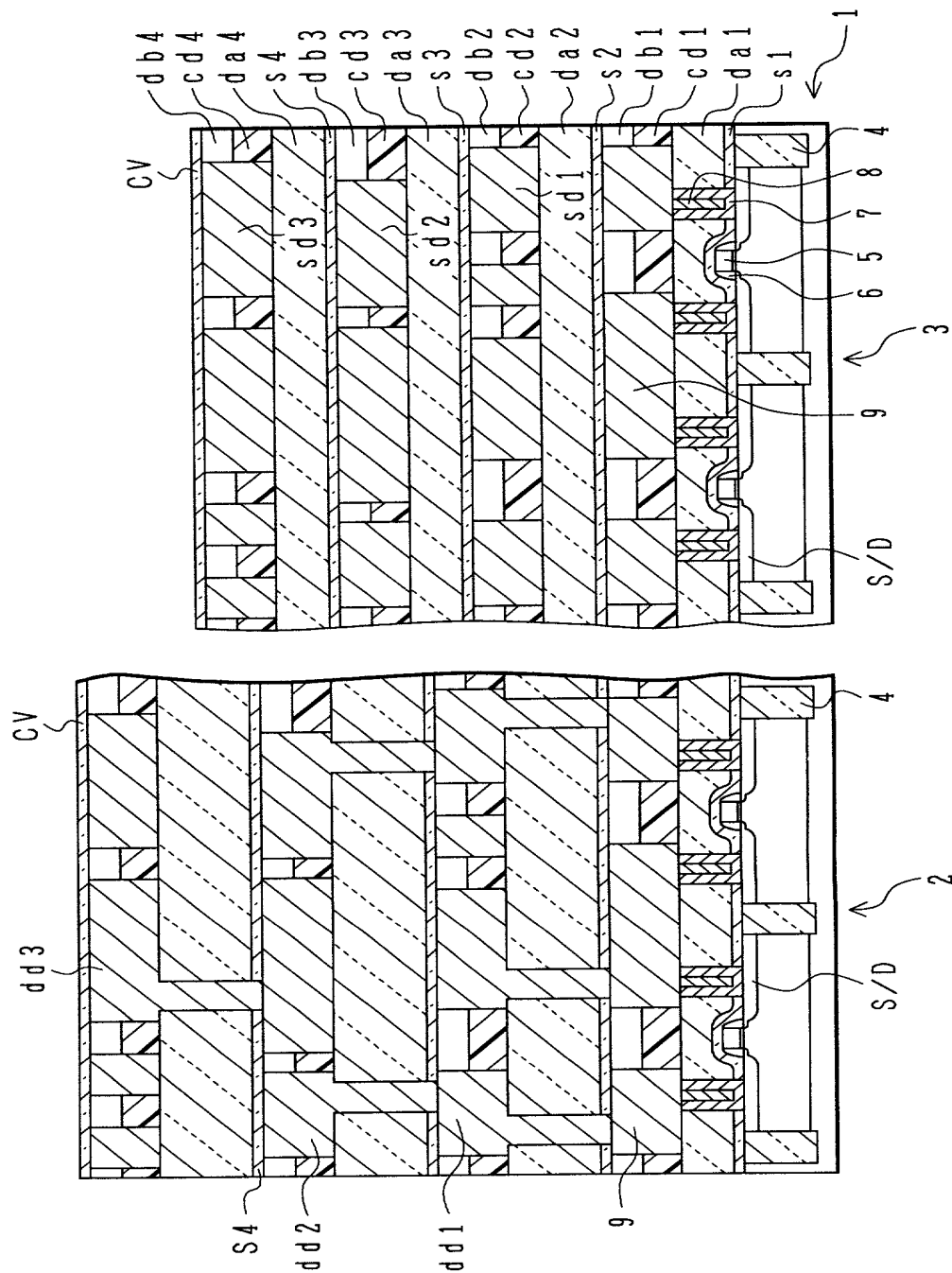


FIG. 4

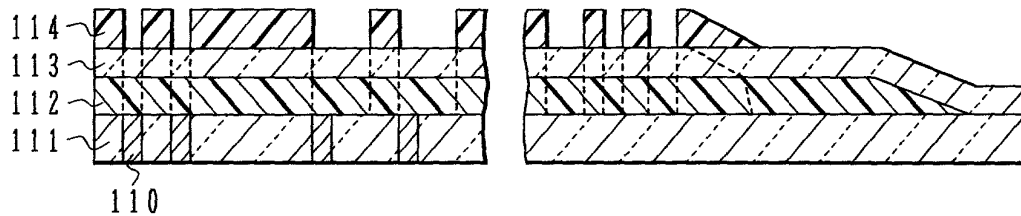


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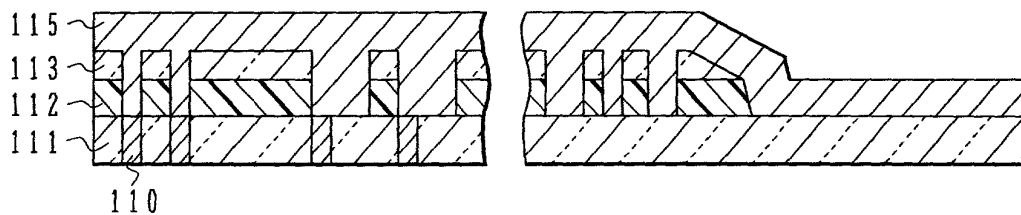
EFFECTIVE WAFER AREA

NONEFFECTIVE WAFER AREA  
(PERIPHERAL WAFER AREA)

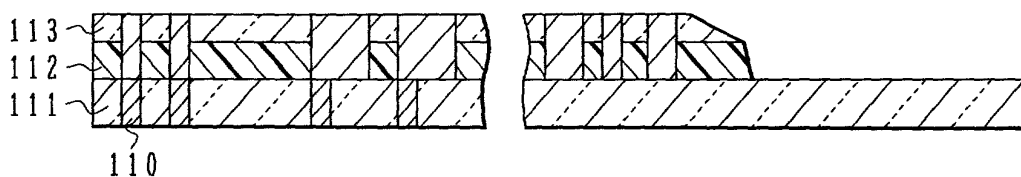
**FIG.5A**



**FIG.5B**



**FIG.5C**



**FIG.5D**

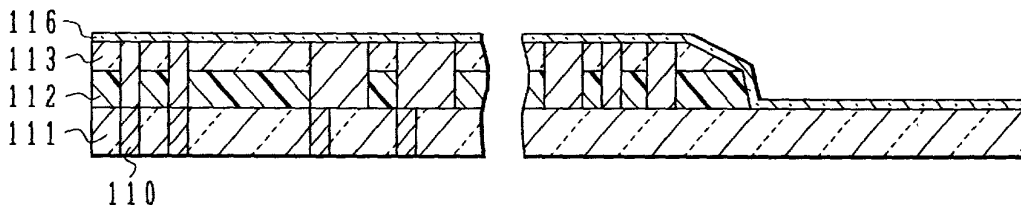
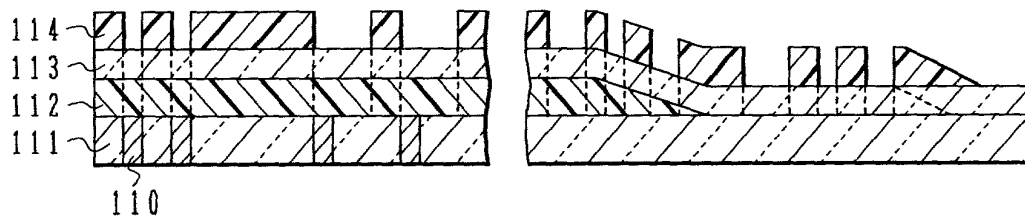


FIG. 6A

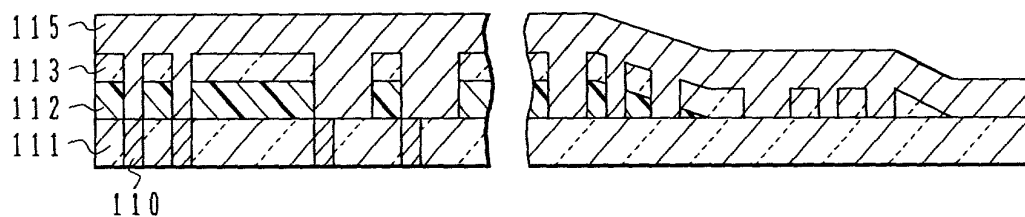
EFFECTIVE WAFER AREA

NONEFFECTIVE WAFER AREA  
(PERIPHERAL WAFER AREA)

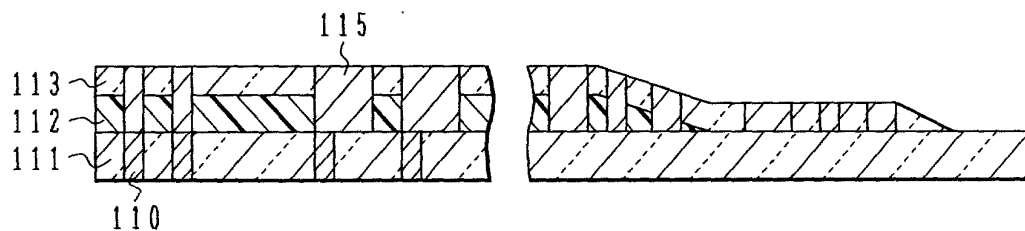
**FIG. 6A**



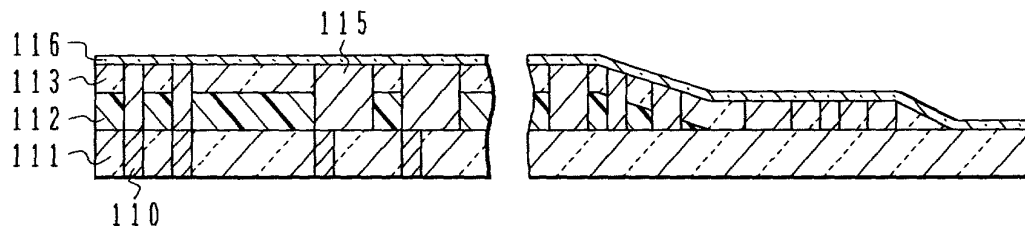
**FIG. 6B**



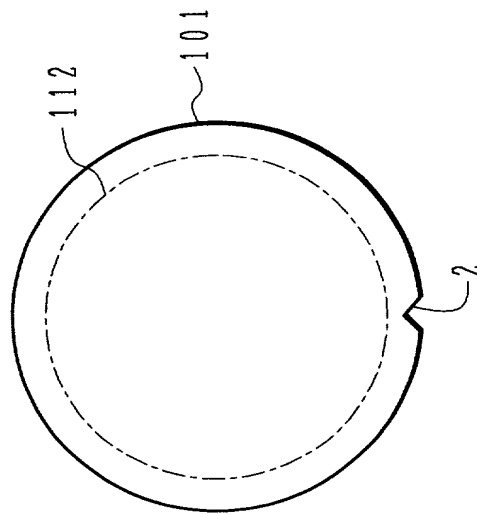
**FIG. 6C**



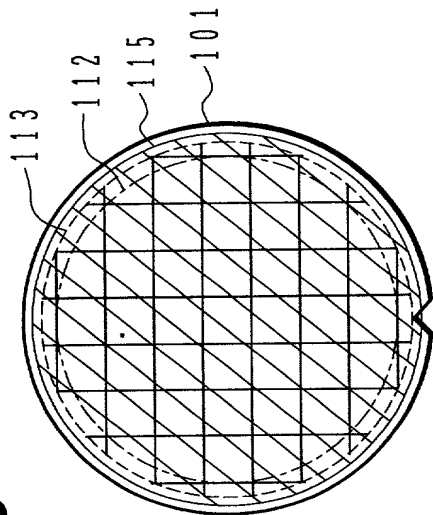
**FIG. 6D**



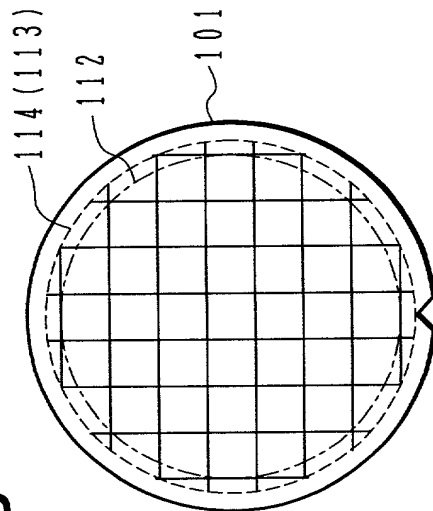
**FIG. 7A**



**FIG. 7C**



**FIG. 7B**



**FIG. 7D**

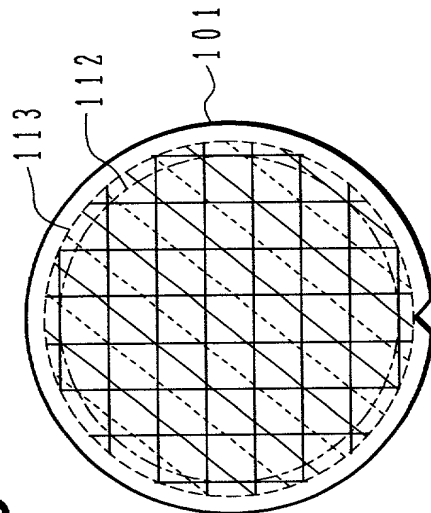


FIG. 8A

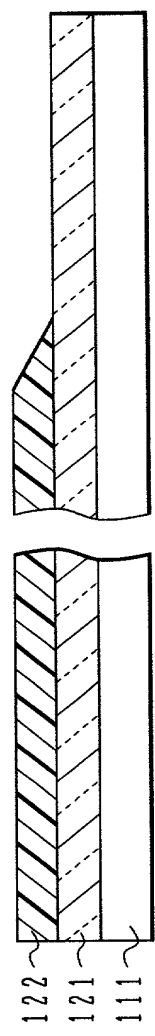


FIG. 8B

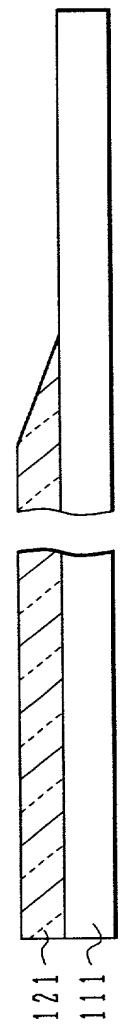
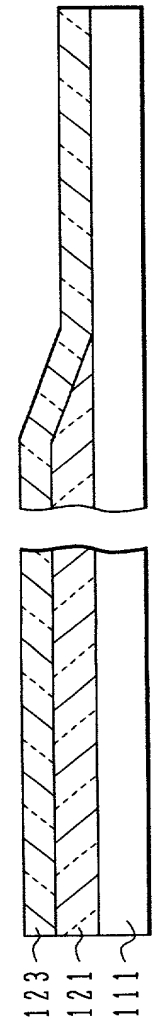


FIG. 8C

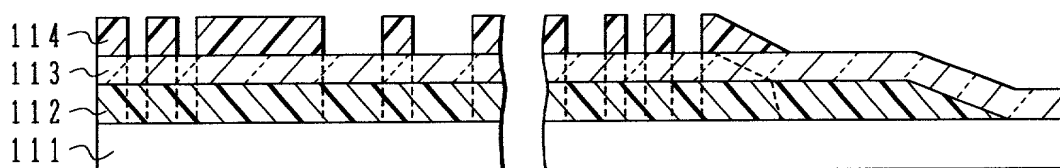


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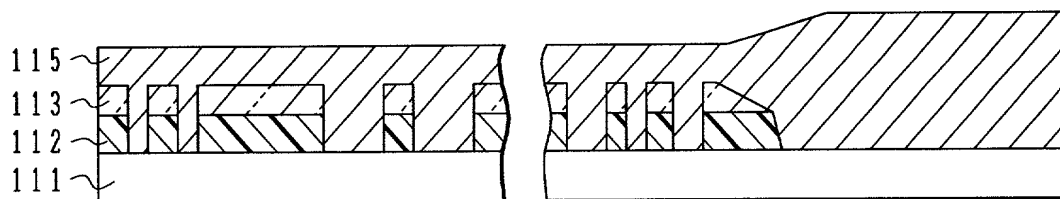
EFFECTIVE WAFER AREA

NONEFFECTIVE WAFER AREA  
(PERIPHERAL WAFER AREA)

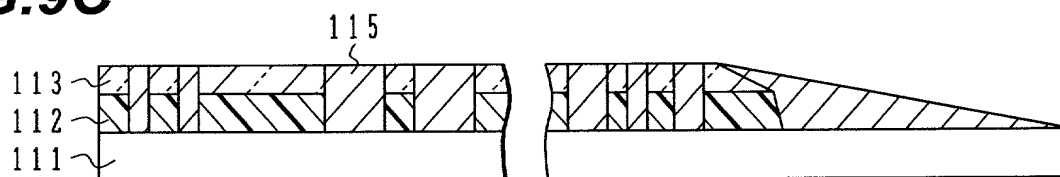
**FIG.9A**



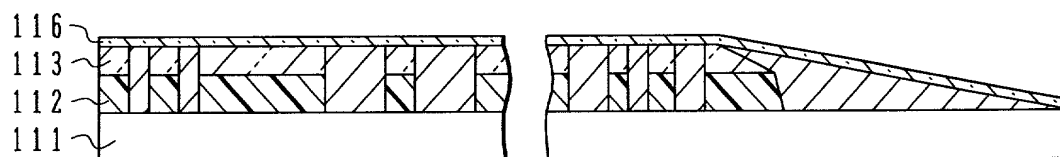
**FIG.9B**



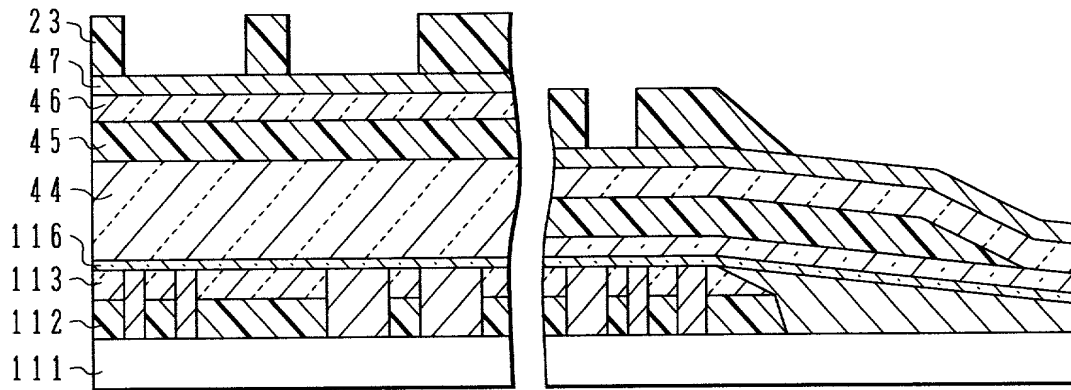
**FIG.9C**



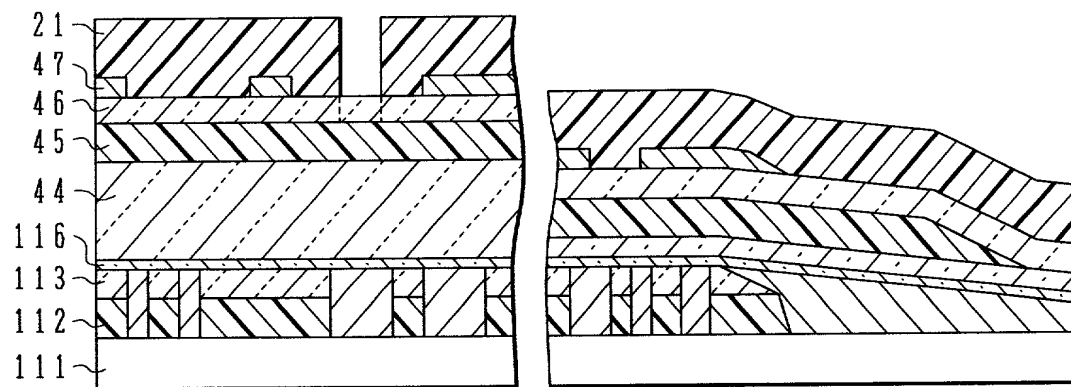
**FIG.9D**



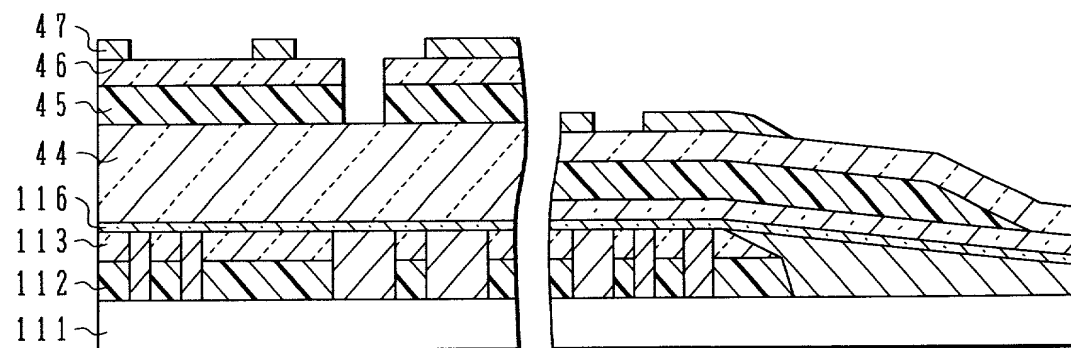
**FIG.9E**



**FIG.9F**

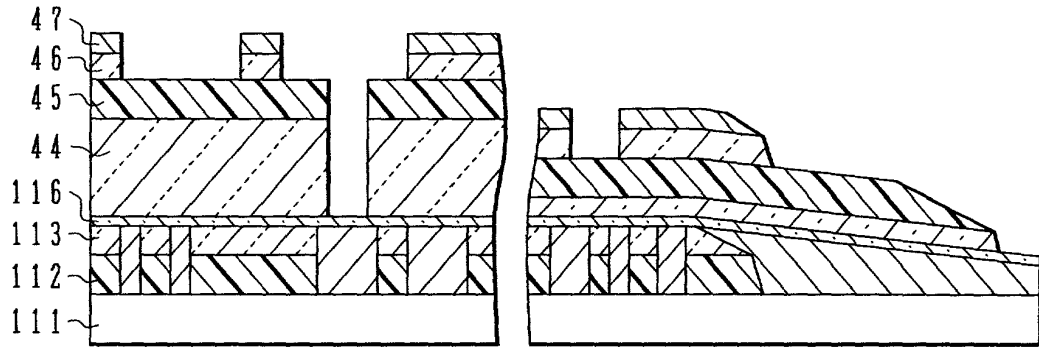


**FIG.9G**

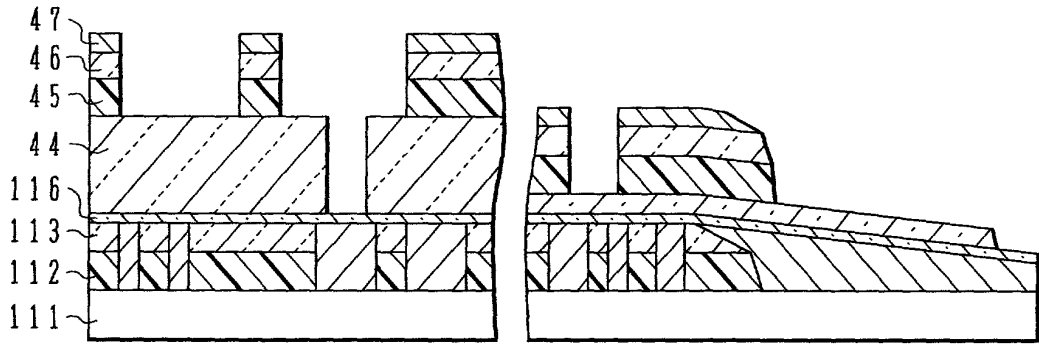




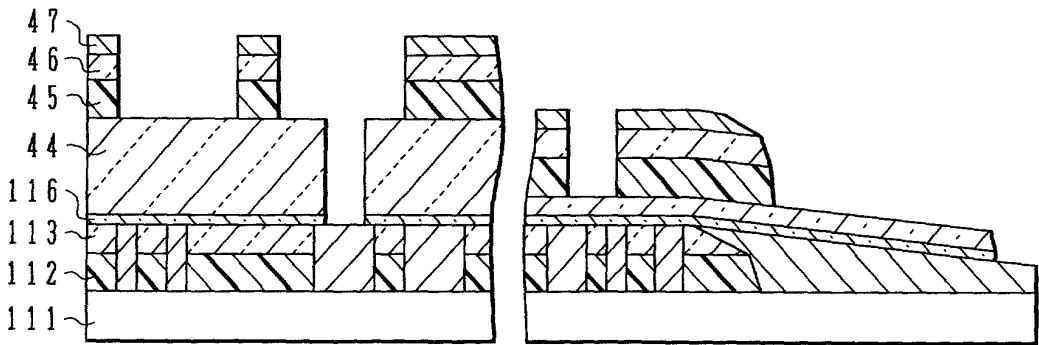
**FIG.9H**



**FIG.9I**

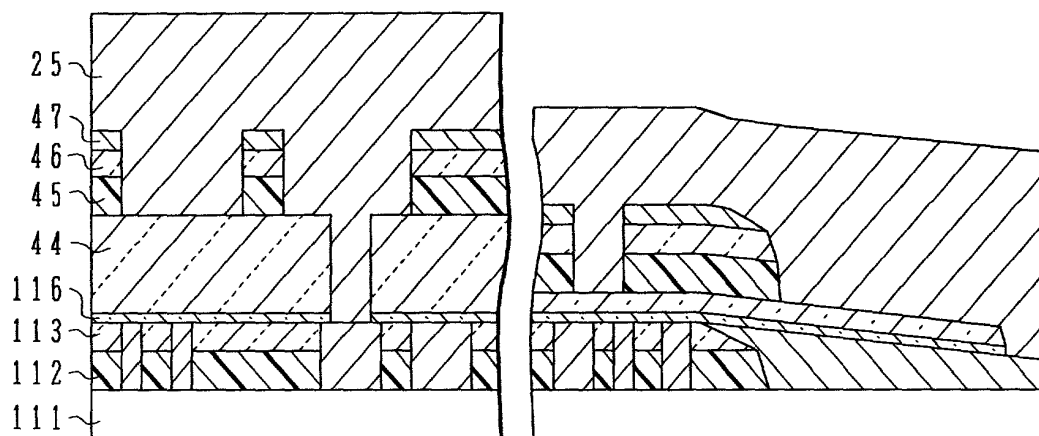


**FIG.9J**

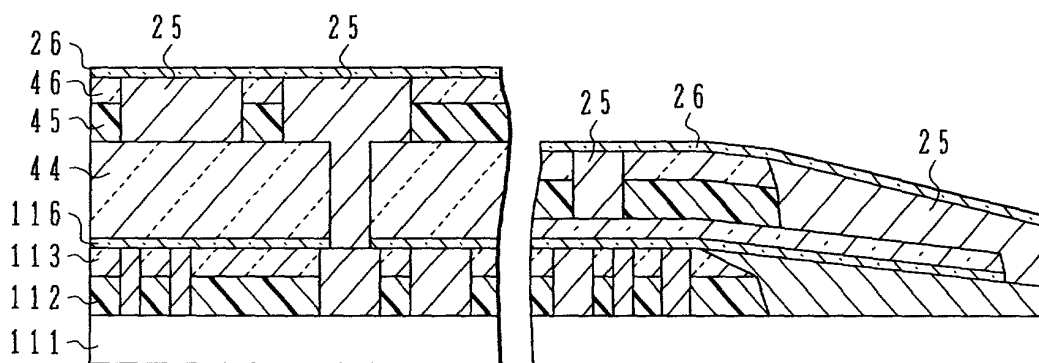


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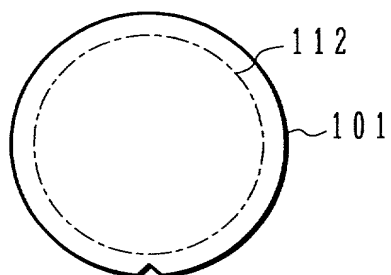
**FIG.9K**



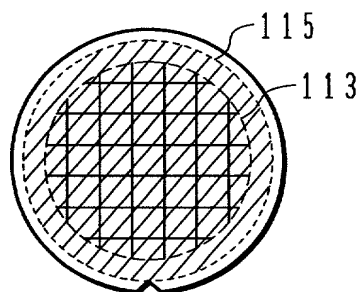
**FIG.9L**



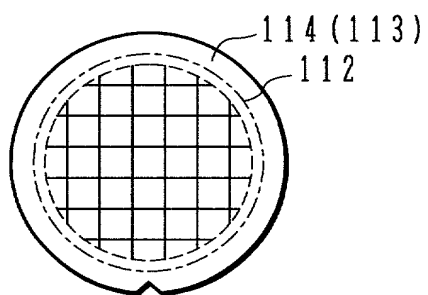
**FIG.10A**



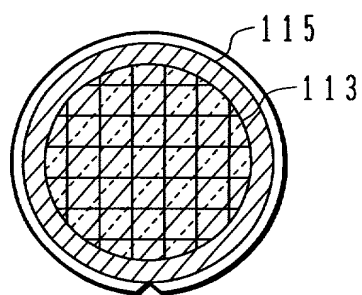
**FIG.10C**



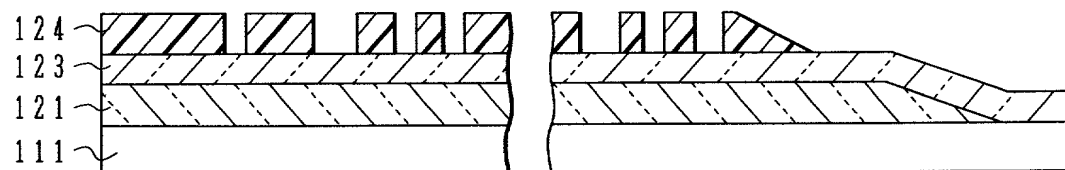
**FIG.10B**



**FIG.10D**



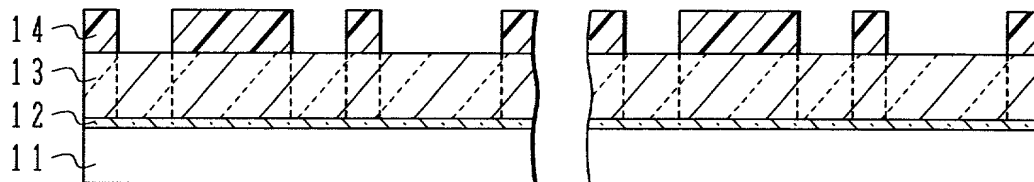
**FIG.11A**



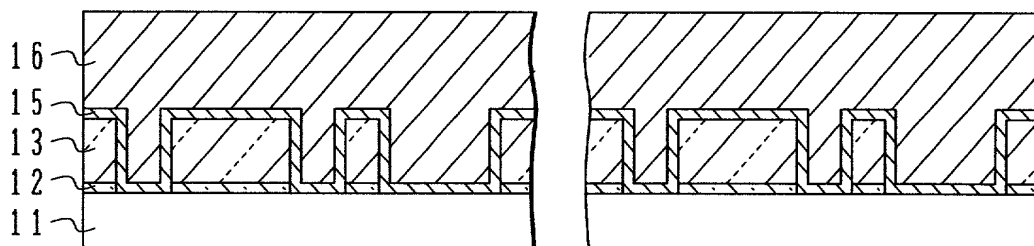
EFFECTIVE WAFER AREA

NONEFFECTIVE WAFER AREA  
 (PERIPHERAL WAFER AREA)

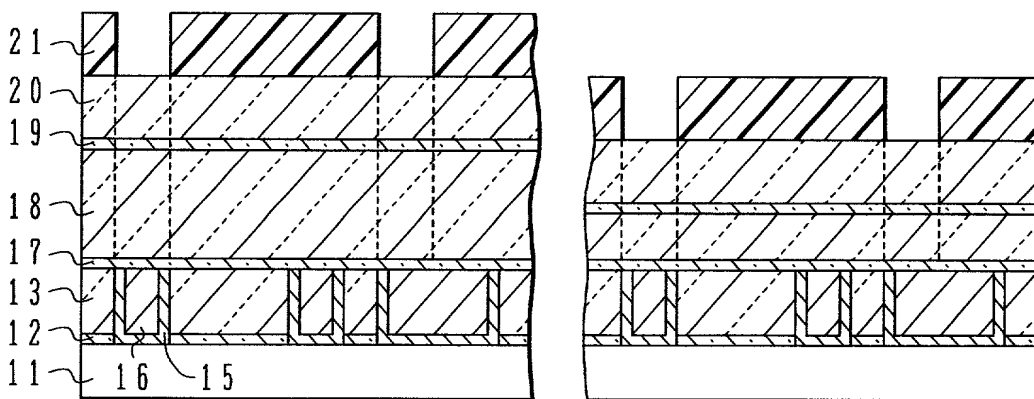
**FIG.12A**



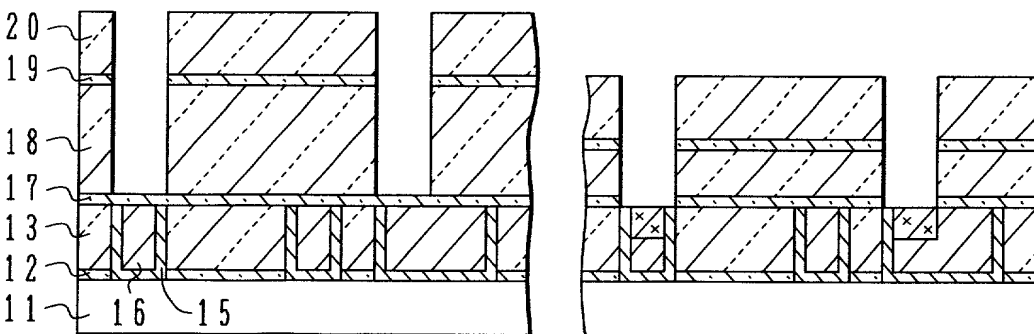
**FIG.12B**



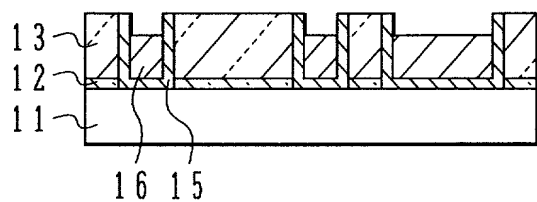
**FIG.12C**



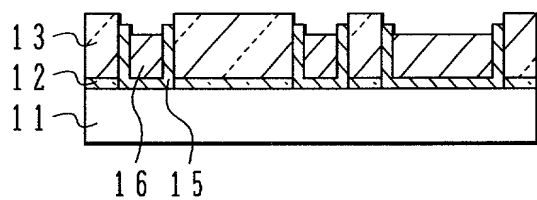
**FIG.12D**



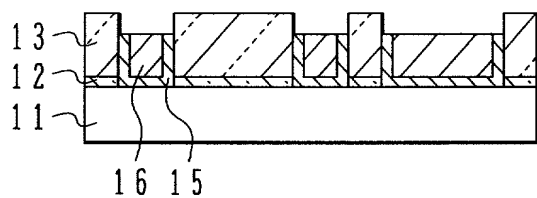
**FIG.13A**



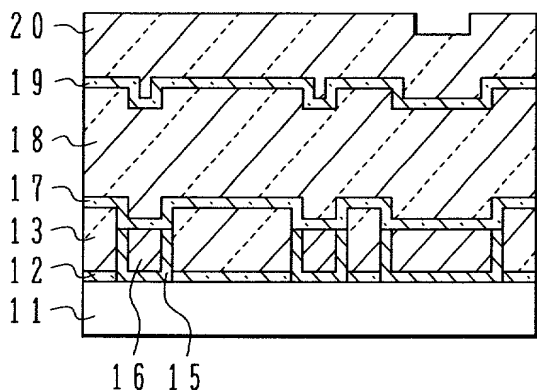
**FIG.13B**



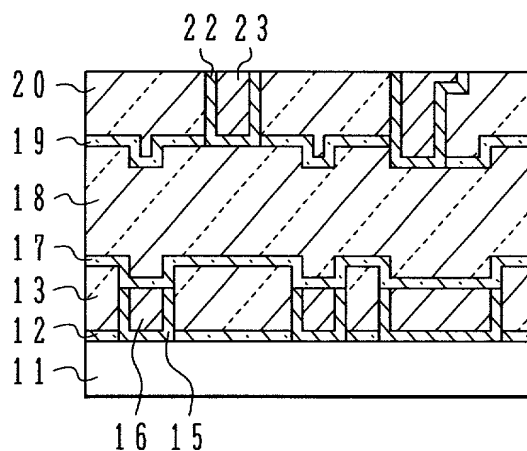
**FIG.13C**



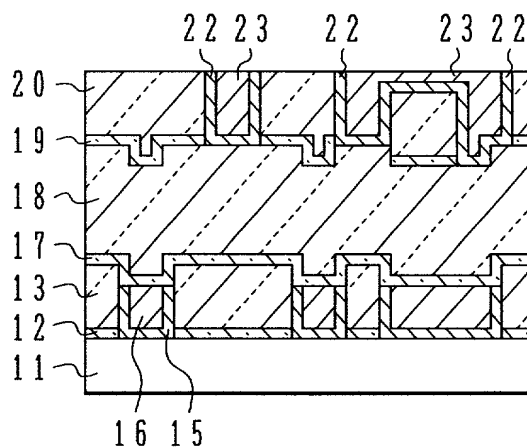
**FIG.13D**



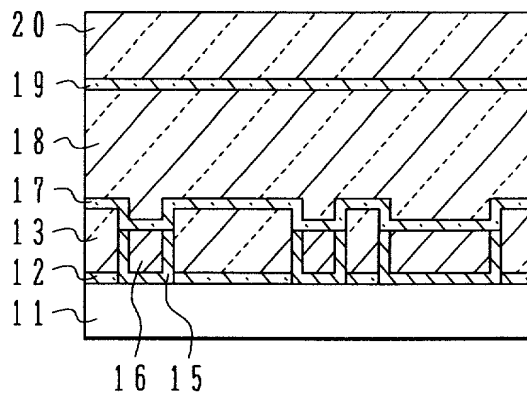
**FIG.13E**



**FIG.13F**



**FIG.13G**

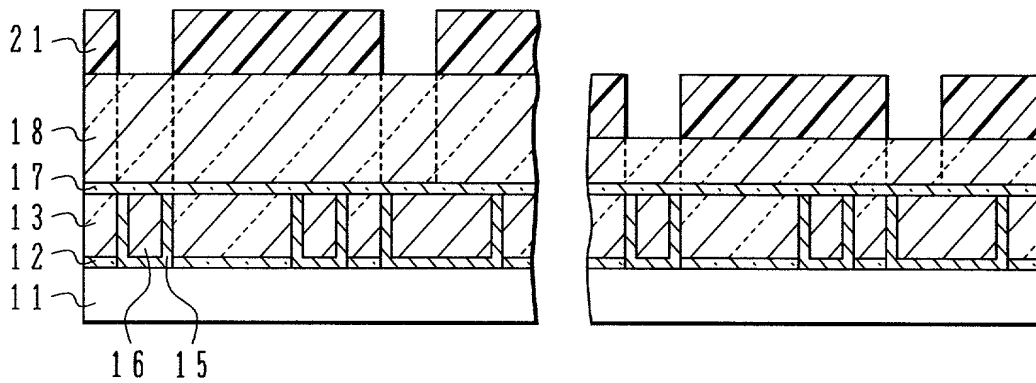


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EFFECTIVE WAFER AREA

NONEFFECTIVE WAFER AREA  
(PERIPHERAL WAFER AREA)

**FIG.14A**



**FIG.14B**

